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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,988	07/31/2002	Xiaoning Nie	1406/52	9022

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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,988	NIE, XIAONING	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/25/02, 5/28/02 and 7/31/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/28/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3 have been examined.

2. Acknowledgement of papers filed: foreign priority documents and amendment on 3/25/2002 and oath and application on 7/31/2002. The papers filed have been placed on record.

Priority

3. Receipt of papers submitted under 35 U.S.C. 119(a)-(d) is acknowledged; the papers have been placed on record in the file. The certified copy of German application 199 45 940.1, filed on 3/25/02, has been received and placed on record.

Specification

4. The disclosure is objected to because of the following informalities: numerous grammatical and typing errors.

5. Instances of such errors include, but are not limited to:

Misspelling of hazard ('harzard'), pages 1, 5, 7 and 10.

English grammar error, page 2a.

With deletion on page 2, the sentence remaining between pages 1 and 2 is grammatically incorrect.

Appropriate correction is required for these and all/any other instances of such errors.

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 1-3 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

9. As per claim 1, 2, and 3, it is unclear how the precondition and post-condition bits (P1 and Q1) are implemented. On page 7, applicant states an instruction "ADD R1, R2, #JMP, ON ZERO," then says it is extended to "P1 ADD R1, R2, #JMP, Q1." It is unclear what happened to the previously stated "ON ZERO," if it was fully replaced by the Q1, if they are equivalent or if was left out.

10. It is shown on page 8, lines 10-15 that some instructions have both P1 and Q1, and some only have Q1, yet no adequate description or explanation is given for how or why this occurs. In fact, Q1 supposedly indicates that "a relative jump is executed if the post-condition flag = 1 and the condition is fulfilled," page 15, lines 15-16. The "'C' program," on page 8, lines 4-7, only necessitates one jump, i.e., (if $A \neq 1$) jump to the 'else' statement. It is unclear and not explained why there are two instructions with the capability to jump (Test and Store both have the post-condition Q1). Also, there is no indication or comment on where the STORE instruction is supposed to jump to, and

since this is the only instruction shown with both a post-condition and precondition, it is assumed this is applicant's claimed processor instruction. Therefore, there is an instruction without a jump address and with both a precondition and post-condition and there is an instruction with a jump address and a post-condition, but no precondition, however there is no instance of the claimed conditional jump instruction with a precondition, post-condition and jump address. There also is no 'L' address shown in the code for the TEST instruction to jump to

11. On page 9, lines 1-21, there a "'C' program" shown that includes an incrementing loop. It is then stated that this code is converted to a "substantially simplified machine program". However, these programs are not logically equivalent. It appears as though the machine program is a decrementing loop, and while the end result may or may not be the same, there is no explanation for the two non-logically equivalent sets of code. Also, there are instructions that are not adequately defined, some instructions have comments after them and some do not. The "STORE_INDEXED" instruction stores a value in an apparent variable "L1", yet the following instruction "DECREMENT" which is assumed to be a conditional jump instruction appears to have it as a jump address. It is unclear whether or not "L1" is a label for a constant address in memory or is a variable. Also, there is again only a post-condition for the conditional jump instruction (DECREMENT), and no precondition is shown, without any explanation. The varying interpretation of "L1", lack of explanation and definition of instructions and inconsistent use of preconditions and post-conditions makes it unclear as to what applicant's machine code is doing or how and why it is being done.

12. On page 9, line 20 to page 10, line 2, applicant provides another unclear example. The pseudo code or 'C" program shown on page 9, lines 31-34, has four instructions with undefined opcodes, labels and variables. These unclear instructions are then simplified into the code on page 10, lines 1-2, presumably with preconditions and post-conditions, since applicant states "according to the invention," yet they are not shown, defined or mentioned. It is unclear how the present invention allows such simplifications.

13. In conclusion, the lack of clarity of these examples and the specification caused by inconsistencies and overall lack of explanation, prevents one of ordinary skill from understanding the post-condition or precondition concept in the conditional jump instruction. There is no shown instance of a conditional jump instruction with a precondition, post-condition and jump address as claimed. The claim(s) therefore contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention without undue experimentation.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahon et al., "Hewlett-Packard Precision Architecture: The Processor", herein referred to as Mahon, in view of Mahlke et al., "A Comparison of Full and Partial Predicated Execution Support for ILP Processors", herein referred to as Mahlke.

16. As per claim 1, Mahon teaches a method for processing conditional instructions in a processor with pipeline architecture, that has the following steps:

a. Loading and decoding a processor instruction (paragraph 3, left column, page 5), the processor instruction (BR instruction) containing an instruction opcode ('opcode' field), register addresses ('r' field), a relative jump distance ('i' field), and a post-condition ('c' field). (Page 20, line 5 and Page 10, right column, 6th full paragraph to page 11, line 6. Also Page 11, left column, 4th full paragraph to end of column.)

b. And jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled: (Page 20, line 5 and Page 10, right column, 6th full paragraph to page 11, line 6. Also Page 11, left column, 4th full paragraph to end of column.)

17. Mahon fails to teach wherein the instruction contains a precondition and the step of the execution of the decoded processor instruction if the precondition is fulfilled.

18. However, Mahlke teaches wherein every instruction contains an additional source operand to hold a predicate specifier (precondition) (Page 139, left column, lines 1-3). If the precondition is true, the instruction is executed, however if it is false, the instruction is not executed. (Page 139, right column, 3rd full paragraph). Mahlke also

teaches that using the predicated method in place of a large portion of branch instructions (i.e., not all) can improve processor performance significantly (Page 139, left column, first full paragraph). It is therefore inherent that there are some unconverted branch instructions that contain a predicate specifier (precondition). Also, a predicated branch instruction is shown in figure 3, under heading 'fully predicated code' and sub-heading 'branch instructions'.

19. The combination of the full predication of Mahlke and Mahon would result in a branch instruction (conditional jump instruction) with a precondition (predicate specifier) and post-condition (c). It would have been obvious to one of ordinary skill in the art to add the full predication of Mahlke to the instruction processing of Mahon because of the improved processing performance it offers. (Page 138, Abstract, final sentence).

20. As per claim 2, Mahon, in view of Mahlke, teaches the method as claimed in claim 1, in which the post-condition comprises a plurality of post-condition bits that are checked in the processor ("BRANCH ON BIT instruction allows branching on the value of any bit in a general register," which constitutes a plurality of post-condition bits that are checked in the processor. (Last paragraph of Page 10 to first paragraph of page 11).

21. As per claim 3, Mahon teaches an apparatus for processing conditional jump instructions in a processor with pipeline computer architecture, having:

-An instruction decoder (paragraph 3, left column, page 5) for decoding a processor instruction (BR instruction) that contains an instruction opcode ('opcode' field), register addresses ('r' field), relative jump distance ('i' field), and a post-condition

('c' field), (Page 20, line 5 and Page 10, right column, 6th full paragraph to page 11, line 6. Also Page 11, left column, 4th full paragraph to end of column.)

-The instruction decoder checking whether the post-condition is fulfilled, driving a program counter for forming jump address as a function of the relative jump distance contained in the processor instruction. (Page 20, line 5 and Page 10, right column, 6th full paragraph to page 11, line 6. Also Page 11, left column, 4th full paragraph to end of column.) Since the instruction fetch unit (instruction decoder) "is responsible for the control flow in the processing of instructions" and because dependent on the post-condition being fulfilled or not, different fetching must occur, it is inherent that it checks whether the post-condition was fulfilled, in order to proceed with proper control flow.

22. Mahon fails to teach the processor instruction containing a precondition and the instruction decoder checking in the case of a fulfilled precondition whether the post-condition is fulfilled and, in the case of a fulfilled post-condition, driving a program counter for forming jump address as a function of the relative jump distance contained in the processor instruction.

23. However, Mahlke teaches wherein every instruction contains an additional source operand to hold a predicate specifier (precondition) (Page 139, left column, lines 1-3). If the precondition is true, the instruction is executed, however if it is false, the instruction is not executed. (Page 139, right column, 3rd full paragraph). Mahlke also teaches that using the predicated method in place of a large portion of branch instructions (i.e., not all) can improve processor performance significantly (Page 139, left column, first full paragraph). It is therefore inherent that there are some

unconverted branch instructions that contain a predicate specifier (precondition). Also, a predicated branch instruction is shown in figure 3, under heading 'fully predicated code' and sub-heading 'branch instructions'.

24. The combination of the full predication of Mahlke and Mahon would result in a branch instruction (conditional jump instruction) with a precondition (predicate specifier) and post-condition (c), wherein the precondition would prevent the conditional jump instruction from being executed if false. It would have been obvious to one of ordinary skill in the art to add the full predication of Mahlke to the instruction processing of Mahon because of the improved processing performance it offers. (Page 138, Abstract, final sentence).

Conclusion

25. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schlansker, U.S. Patent 5,999,738. The prior art teaches a processor that uses predicates.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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